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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,570	06/24/2003	Mikhail I. Grinchuk	01-1060/L13.12-0207	1724

7590 02/24/2005

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EXAMINER	
LIN, SUN J	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,570	GRINCHUK ET AL.	
	Examiner	Art Unit	
	Sun J. Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,12 and 13* is/are rejected.

7)☒ Claim(s) *2-11 and 14-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/24/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/602,570 and preliminary amendment filed on 06/24/2003. Claims 1 – 22 remain pending in the application.

Claim Objections

2. Claims listed below are objected to because of the following informalities:

Claim 1, line 1, change "logic circuits" to **—a logic circuit—**.
Claim 1, line 7, before "number" delete **—the—**.
Claim 1, line 7, change "variables to" to **—variables of—**.
Claim 1, line 10, before "value" delete **—a—**.
Claim 2, line 6, before "circuit" insert **—logic—**.
Claim 2, line 8, before "number" delete **—the—**.
Claim 4, line 5, before "number" delete **—the—**.
Claim 8, line 5, before "number" delete **—the—**.
Claim 13, line 9, before "number" delete **—the—**.
Claim 13, line 12, before "number" delete **—the—**.
Claim 13, line 13, change "integer;" to **—integer; and—**.
Claim 13, line 15, before "two-input" insert **—the—**.
Claim 13, line 15, before "gates" insert **—AND and OR—**.
Claim 13, line 16, before "value" delete **—a—**.
Claim 13, line 16 – 17, delete **—between 3^n and ... an integer—**.
Claim 14, line 2, change "including steps of" to **—including—**.
Claim 15, line 2, change "including steps of" to **—including—**.
Claim 17, line 2, change "including steps of" to **—including—**.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1, 12 and 13 are rejected under 35 U.S.C. 102(a) as being unpatentable over IEEE paper entitled "*Timing-Driven Logic Bi-Decomposition*" authored by *Cortadella*.

5. *Cortadella* shows and teaches the following subject matter:

- An *approach* (i.e., *process*) of finding *minimum-depth tree* (i.e., logic depth reduction) – [page 676, left column];
- A *process* for *logic decomposition* (i.e., *logical operation*) of a logic circuit to achieve *tree-height reduction* based on a function F = a **AND** (b **OR** (c **AND** (d **OR** (e **AND** (f **OR** (g **AND** h)))))) – [page 676; Section II. Overview; Fig. 2(a)];
- Selecting N (=8) as number of variables of the logic circuit – [Fig. 2(a)];
- Implementing the logic circuit with two-input gates (i.e., **OR**-gates and **AND**-gates) to a depth d = 4 between 2n and 2n + 2 [i.e., $2n \leq d \leq (2n + 2)$] based on a value of N (i.e., N = 4) between 3^n and 3^{n+1} [i.e., $3^n \leq N \leq 3^{n+1}$], where n = 1 – [Fig. 2(d)].

For reference purposes, the explanations given above in response to Claim 1 are called **[Response A]** hereinafter.

6. As to Claim 12, *Cortadella* shows in Fig. 2 and teaches the subject matter in Section II. Overview.

7. As to Claim 13, in addition to reasons included in **[Response A]** given above, *Cortadella* also teach that the *tree-height reduction* was originally proposed in the scope of optimizing compilers for generation of *code* in multiprocessor systems – [Section II. Overview]. Notice that (1) the number of inputs N can be evaluated by a first computer code (2) the logic circuit with two-input **AND** and **OR** gates can be implemented using a second computer code.

Allowable Subject Matter

7. Claims 2 – 11 and 14 – 22 are objected to as being dependent upon a rejected base claim, but they would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Those claims are allowed is because that the prior art does not teach or fairly suggest the following subject matter:

- A process of implementing a logic circuit for logical operations based on a function as recited in Claim 1 comprising a step of defining a *top portion* defining at least a *top level* of the of the logic circuit and having **N** inputs and N/3 outputs in combination with other limitations as recited in **Claim 2**;
- A process of implementing a logic circuit for logical operations based on a function as recited in Claim 1 comprising a step of transforming groups of three variables of the function into new groups having at most two variables each in combination with other limitations as recited in **Claim 3**;
- A process of implementing a logic circuit for logical operations based on a function as recited in Claim 1 comprising a step of, for a predetermined value of **N**, designing a first logic circuit having **N – 1** inputs and a pre-selected pattern of first and second gate type, the first logic circuit having a portion receiving **I – 1** most significant input where I is a smaller than **N – 1** in combination with other limitations as recited in **Claim 7**;
- The process of Claim 1 further including steps of *designing*, *setting* and *removing* as recited in **Claim 11**;
- A computer useable medium of Claim 13 further includes *third computer code*, *fourth computer code* and *fifth computer code* in combination with other limitations as recited in **Claim 14**;
- A computer useable medium of Claim 13 further includes *third computer code*, *fourth computer code*, *fifth computer code* and *sixth computer code* in combination with other limitations as recited in **Claim 15**;
- A computer useable medium of Claim 13 further includes *third computer code* and *fourth computer code* in combination with other limitations as recited in **Claim 17**;

- A computer useable medium of Claim 13 further includes *third computer code*, *fourth computer code*, *fifth computer code* and *sixth computer code* in combination with other limitations as recited in **Claim 20**.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J Lin whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (571) 272 - 1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sun James Lin
Patent Examiner
Art Unit 2825
February 22, 2005